VLSI Final Exam (Cmpt 421.3 and 814.3)

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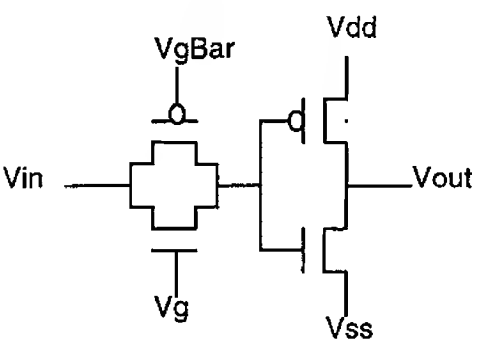
This exam consists of ten short questions (worth 5 points each) and one long question regarding the design of a VLSI application (worth 50 points). Feel free to give point-form answers to questions, instead of writing complete sentences and paragraphs.

1) [5] Describe the physical basis of silicon pn-junction diodes. Explain the electrical properties of this structure. Explain how these diodes can be dynamically and temporarily overridden.

2) [5] What are the principle factors which tend to limit the density of CMOS devices? What are the principle factors which tend to limit the physical size of chips?

3) [5] Draw a Vin / Vout transfer characteristic for a CMOS inverter. Identify and explain the reasons for the regions of maximal and minimal power consumption. Illustrate the unity-gain points, and explain their significance.

4) [5] Consider the following dynamic latch. Where is the memory stored? What factors affect the set-up time of this latch? What factors affect the hold time of this latch? Can you reduce either set-up or hold time while holding the other constant? Why?, why not?



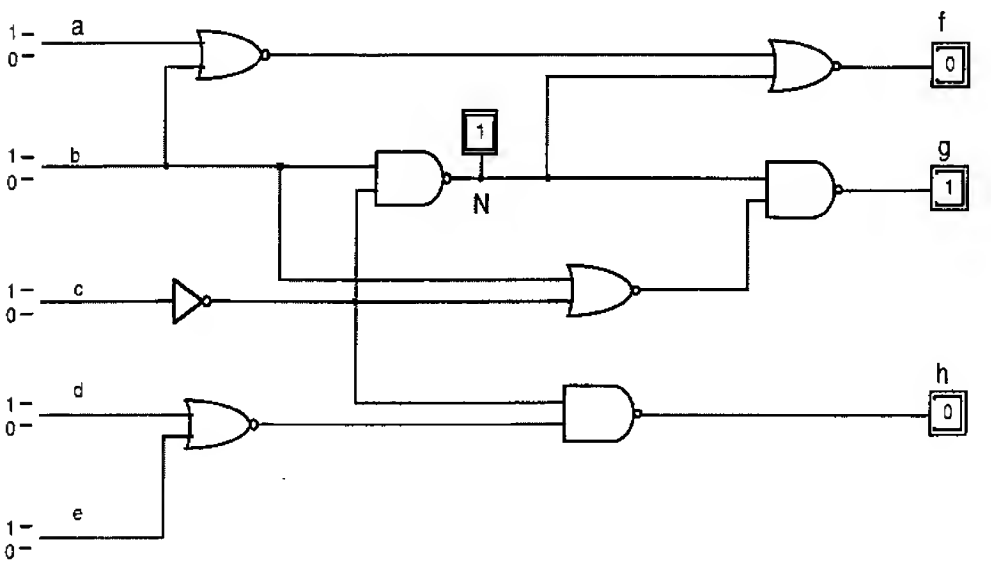
5) [5] Sketch a two stage Zipper CMOS gate for the function *A nor (B nand C)*. Briefly explain its operation.

6) [5] Design an nMOS PLA for the following two functions:

f = ~a*~c + a*b
g = a*b + ~a*c + ~b*~c

Give a transistor level circuit for this PLA.

7) [5] Find a test vector to test for a stuck-at-0 at node N in the following circuit.



8) [5] Explain the division of work between placement and routing. Why must (reasonable) placement involve some aspects of routing. Name and describe an algorithm for switch-box routing.

9) [5] Describe, briefly, the architecture of a typical SRAM-based FPGA. Describe the typical steps required to implement some logical system on an FPGA.

10) [5] What VLSI problem does the Penfield-Rubinstein model address? Describe the problem, describe the P-R model, and indicate how the P-R model differs from other models relevant to the problem.

11) [50] As a high-level VLSI design engineer, you've been given the job of preparing a preliminary design document for the following problem:

A system requires the ability to receive 32 bit messages (which are to be called "infolets") from a number of very high speed devices. Each infolet source generates infolets intermittently. All of these infolets must be concentrated to be processed at one place. Higher level architects than you have decided to use a 2-to-1 queueing multiplexer for this purpose; 2^n-1 of these devices will be assembled into a binary tree with sources as leaves and the root as the infolet receiver. Your job is to design this 2-to-1 Mux.

The Mux will have two infolet inputs (A and B), one infolet output (C), and signals to indicate the presence of infolets on the inputs and the output on any particular clock cycle (AP, BP, CP).

As the inputs can provide twice the infolet volume that the output can dispose of, it is necessary to provide internal queue space to smooth the infolet flow in case of input bursts. The Mux will contain queue space for 128 infolets, which will be organized as a fifo (when both A and B have infolets on any cycle, alternate priorities between the two ports).

Of course the 128 infolet queue can overflow. When this happens, turn on an error signal (E) and discard of the lowest priority input.

On each clock tick, the Mux should be capable of receiving and disposing of infolets on all ports, and of leaving its internal registers in a correct state for the next cycle.

Your assignment is to proceed in a top-down fashion toward a design for this problem. At each level of design, consider (and state) the alternatives, and their advantages and disadvantages. Make choices among these alternatives, and proceed to the next sub-problem. Indicate how choices in one area affect another area. Focus your efforts on the many VLSI issues raised by this problem.

There is no particular right answer to this question. It is intentionally a very open-ended opportunity for you to display the breadth of your knowledge of VLSI systems.

Good luck, and Merry Christmas!